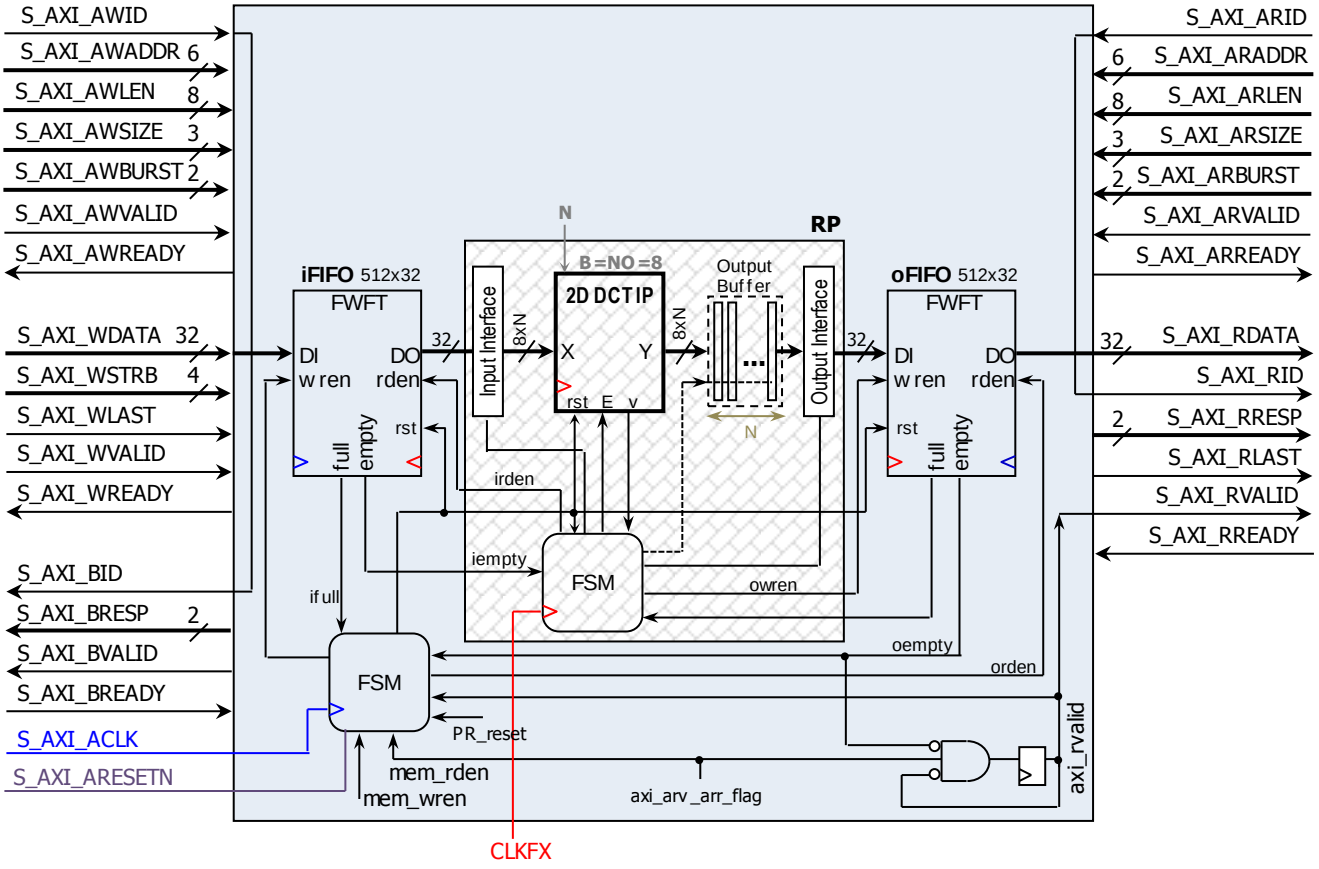
Homework 4

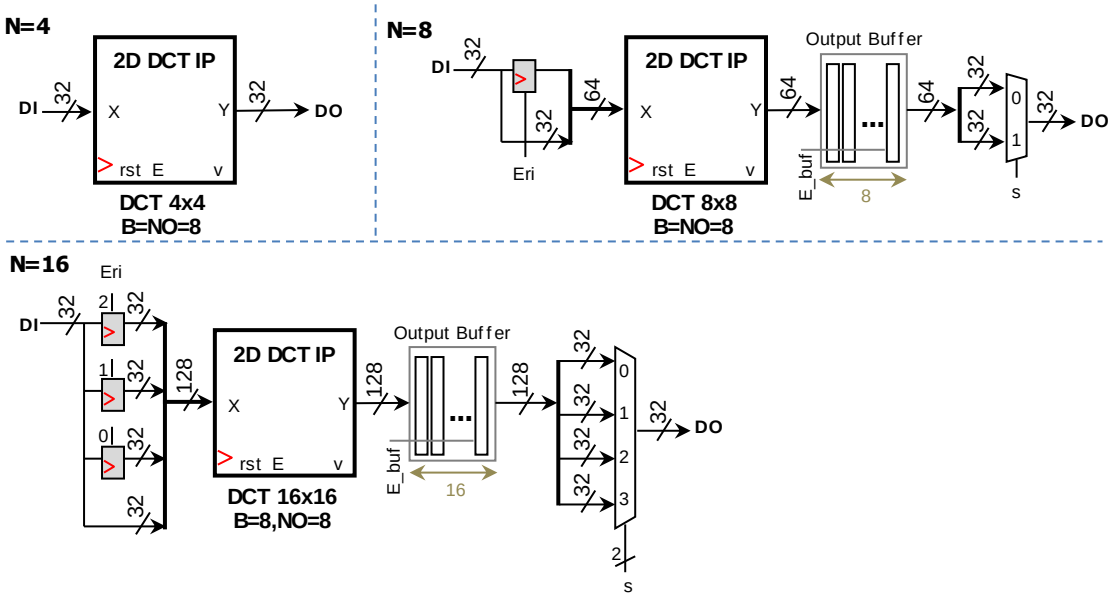
(Due date: November 26th @ 5:30 pm)

PROBLEM 1 (15 PTS)

- The figure shows the 2D DCT IP AXI4-Full interface. It also shows a Reconfigurable Partition (RP). We allow for N to be run-time reconfigurable ($N = 4,8,16$), and we fix the parameters $B = NO = 8$.



- The input and output might require more than 32 bits. In this case, we need an input interface to the iFIFO and output interface to the oFIFO. The figure shows the different interfaces for each N (4, 8, 16) when $B = NO = 8$. The FSM @ CLK_FX controls data flow from the input and the output, and as such, it depends on N.



- We want to build a dynamically reconfigurable system, where we can change N (4,8,16) at run-time:
  - ✓ The RP (Reconfigurable Partition) is indicated in the figure. The input interface and the output interface to FIFOs, as well as the FSM @ CLK_FX are included in the RP. Why is this necessary?
  - ✓ Signal rst: Generated by the FSM @ S_AXI_ACLK. It resets the 2D DCT IP, the red FSM, and the FIFOs. Why is this signal important? Do we assert this signal before or after performing DPR? Why?
  - ✓ The RP outputs toggle during DPR. What could happen to the contents of oFIFO during DPR?

PROBLEM 2 (85 PTS)

- Attach a printout of your Project Status Report (no more than 2 pages, single-spaced, 2 columns). This report should contain the current status of your project. You **MUST** use the provided template (`Final Project – Report Template.docx`).
  - ✓ Include a Block Diagram of your system.
  - ✓ Specify clearly the allocation of tasks in i) reconfigurable hardware, and ii) software routine.